Low Cost COTS Radar

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Abstract

This paper describes the low cost COTS (commercial off the shelf) radar designed by a team of colleagues at SRC, Inc. as an entry to the IEEE Antennas and Aerospace Systems Society (AESS) Radar Challenge [1] to be held at the 2020 IEEE International RADAR Conference [2]. Our goal is to improve upon the signal processing for a COTS mmWave radar built by Texas Instruments.

The Challenge

The AESS Radar Challenge requires entrants to construct a "home brew" radar made from COTS materials that is able to sense multiple targets in a room concealed behind a curtain. The goal is to detail the scene as accurately as possible.

The targets will be a mix of stationary and moving objects, expected to include calibration spheres and corner reflectors. The room has dimensions of 20m x 8m. The curtain will be as transparent as possible in the RF bands while being highly opaque to light. The radar must measure relevant parameters for a small number of targets. Parameters include location, separation distance and speed, for targets in motion. [1]

The LCCR Radar Category

The team is designing a low-cost COTS radar (LCCR) and plans to offer an entry in the Maximum Value Radar category for COTS Bill of Material (BOM) costing less than $750. However, as a backup option, the team may need to enter its candidate in the State of the COTS Art Radar category instead, for BOM cost greater than $750 and less than $3,000. The deciding factor will be the success in implementing a less expensive board to transfer I/Q data from the sensor to the laptop. The options are noted in the BOM.

The LCCR Hardware

The team selected the Texas Instruments IWR1843 single-chip millimeter wave (mmW) sensor [3] which integrates digital signal processing (DSP) [4], micro-controller unit (MCU) [5] and hardware accelerator (HWA) [6]. This industrial radar sensor uses frequency modulated continuous wave (FMCW) technology and operates in the 76 GHz to 81 GHz radio frequency (RF) band with up to 4-GHz continuous chirp. The IWR1843 chip RF and analog baseband signal chain includes the synthesizer, power amps (PA), low noise amps (LNA), mixer, intermediate frequency (IF), and analog-to-digital converter (ADC) blocks for three transmitters and four receivers. Two transmit channels can be used simultaneously for transmit beamforming, and each transmit chain can deliver a maximum of 12 dBm at the antenna port on the PCB. All four receive channels can be used simultaneously and the device supports a complex baseband architecture, designed for fast chirp systems. Each receiver channel has a quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 10 MHz. [3, p.58] **Figure 1** shows the DSP, MCU, and RF and Analog subsystems with external interfaces. **Figure 2** provides a more detailed functional block diagram.

For fast implementation, the team has purchased the Texas Instruments evaluation module (EVM) IWR1843BOOST [7]. The board has an IWR1843 chip mounted along with the additional components needed to facilitate development and a software development kit (sdk) [8] to get started. **Figure 3** is a block diagram of the EVM [9, p.5]. **Figure 4** shows the IWR1843BOOST top side with key parts labeled [10], and **Figure 5** shows the bottom side [9].

The team selected the Texas Instruments DCA1000EVM data capture card [11] to interface with the IWR1843BOOST EVM. A ribbon cable is provided with the data capture card to attach to the EVM's 60-pin Samtec high density connector. **Figure 6** shows the DCA1000EVM functional block diagram [12, p.4]. **Figure 7** and **Figure 8** show the DCA1000EVM top and bottom sides, respectively [12, p.5]. **Figure 9** shows front and side views of the DCA1000EVM and IWR1843BOOST mounted together with ribbon cable connection between the two boards' top sides [12, p.7].

The DCA1000EVM data capture card is the most expensive item in the BOM. To reduce the cost of the LCCR, the development will progress with two parallel efforts. One effort will be to optimize the FMCW techniques to improve performance over the baseline performance available using the software in the SDK. A parallel effort will investigate a significantly lower cost solution using a MYIR Z-turn Lite solution [13]. The Z-turn Lite is a Linux single board computer (SBC) using a 667MHz Xilinx Zynq-7007S system-on-chip (SoC) with a single-core ARM Cortex-A9 processor and integrated Artix-7 Field Programmable Gate Array (FPGA) logic. **Figure 10** shows the MYIR Z-turn Lite top side with some key components labeled and **Figure 11** shows the bottom side. [15]

FCC Compliance

The TI Radar selected operates in the band from 76-81GHz with a transmit power of 12dBm. There are two different kinds of radars operable in that band under FCC rules. In FCC part 15.256, level probing radars are permitted at a peak EIRP of 34 dBm. Additionally, FCC part 95 subpart M defines the use of 76-81 GHz unlicensed operation of radars by any person as long as the device has an EIRP less than 50dBm. Federal Register Volume 82 states "In addition, the amended rules [permitting the use of 76-81GHz for radar] allow for the continued shared use of the 76-81 GHz band by other incumbent users, including amateur radio operators and the scientific research community."

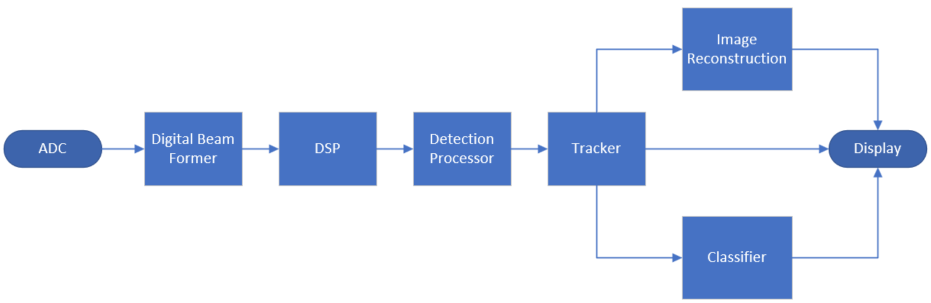
Target Properties

According to the competition guidelines, an operator using the radar should be able to describe the scene behind a curtain which includes calibration spheres and corner reflectors that are both moving and non-moving. Out of the box, the TI radar can measure range-doppler and estimate angle of arrival. Properties of the targets include type (sphere or corner reflector), x,y,z position, and x,y,z velocity. We intend to improve detection of x,y velocity and range through three main methods: implementing Synthetic Aperture Radar, beamforming, and utilizing custom waveforms for improved stretch-processing. A stretch goal is to describe z position of targets by moving the radar vertically on a rail. Further, we would like to eventually use SAR to map both static and moving targets simultaneously. We also intent do use our own signal-processing pipeline, pulling IQ data straight from the ADC.

Theory Of Operation

The LCCR system is made with the intent of surveying a moderately sized room through a combination of electronic beam steering in azimuth dimension and Synthetic Aperture Radar (SAR) in the Z-dimension. This information will then be mapped in relation to the position of the system creating an image of the environment in cylindrical space. Moving Targets will receive additional processing in the form of tracking and classification and be mapped onto the surveyed environment.

The team plans to implement new waveforms and a new Signal Processing Chain to fit the needs of the competition. The Signal processing chain will contain a total of 6 individual elements: digital beamformer, the digital signal processor, detection processor, tracker, classifier, image reconstruction. The following gives a brief description each component:



Waveforms

A staggered set of FMCW waveforms will be used for detection in this system for improved resolution of targets. The waveforms will be designed with the intention of maximizing range resolution for image reconstruction and capturing minimal detectable radial velocity (MDRV) similar to those found common household items. In addition, this set of waveforms will be tuned to minimize the clutter of a room 20 meters wide and 8 meters in length - assuming there are no sources of interference.

Digital Beamformer

The digital beamformer will be used to create beams and from the raw data stream that feeds into the system. The digital beamformer also will form the electronically steered receive beams and output the data into the Digital Signal Processor. The various channels will be converted into single channel.

Digital Signal Processor

The Digital Signal Processor (DSP) will take the received beams and perform doppler processing to resolve targets and mitigate noise. The Digital Signal Processor will also remove clutter and false alarms via the use of a Clutter Map, Range Constant False Alarm Rate (RCFAR) Detector, and Doppler Constant False Alarm Rate (FCFAR) Detector. These detections are outputted into the Detection Processor.

Post Detection Processor

The Post Detection Processor (PDP) will resolve the azimuth and height of the detection. The PDP will also filter out extraneous detections from the DSP. The PDP will contain multiple filters such as the Range Sidelobe Filters, Doppler Sidelobe Filters, Spatial Apodization Filters, etc. These filters will be used to improve the definition of the intended target. All filtered detections will then proceed onto the Tracker and Image Reconstruction.

Image Reconstruction Module

The Image Reconstruction Module (IRM) will produce an image of the static environment using SAR. All detections that are static or close to static will be recorded by the IRM and map to create a model of the surrounding environment. All targets in motion will not be captured through the IRM unless under a certain MDRV threshold. The model of the static environment will be displayed via the display screen.

Tracker

The Tracker will contain a list of tracks. These tracks will capture and store the movement of all targets in the scanned area. Tracks will be displayed alongside the static environment via the display screen. Information on tracks will be fed to the classifier and processed accordingly.

Classification

The classifier will assign a label to all tracks in the tracker. The classifier will use a trained machine learning algorithm to assign a label to the track. The algorithm will be trained on a variety of common household items. This algorithm is not intended to be used on static objects in the environment. Classification labels will be displayed on the display screen.

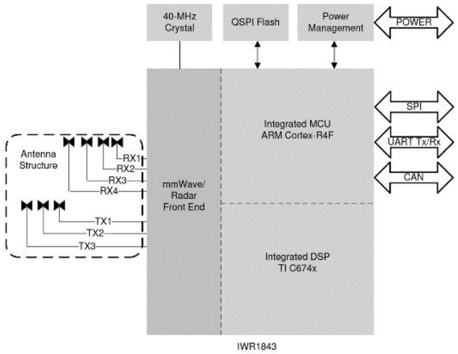


Figure 1: IWR1843 subsystems with external interfaces

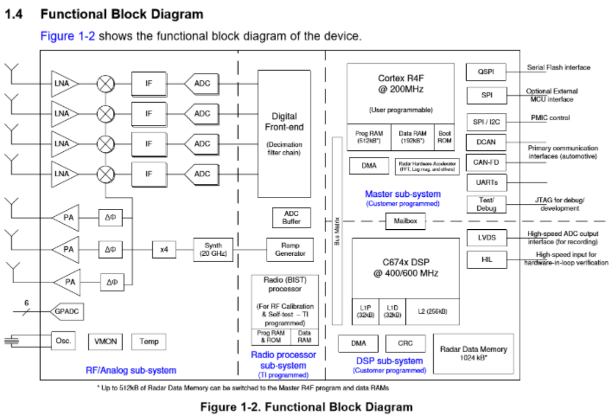


Figure 2: IWR1843 functional block diagram

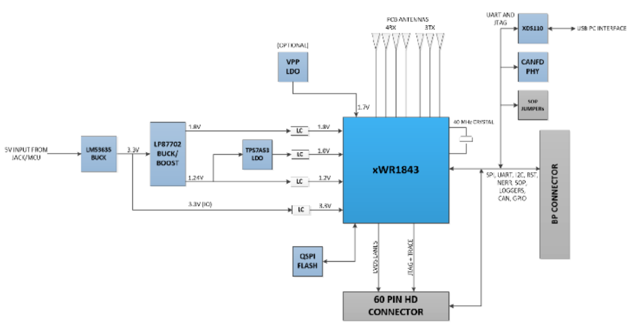


Figure 3: IWR1843BOOST block diagram

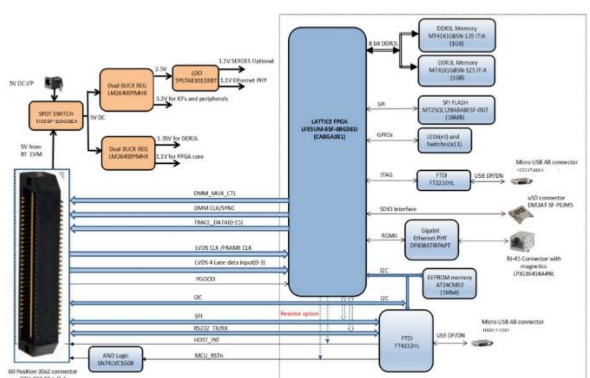


Figure 6: DCA1000EVM functional block diagram

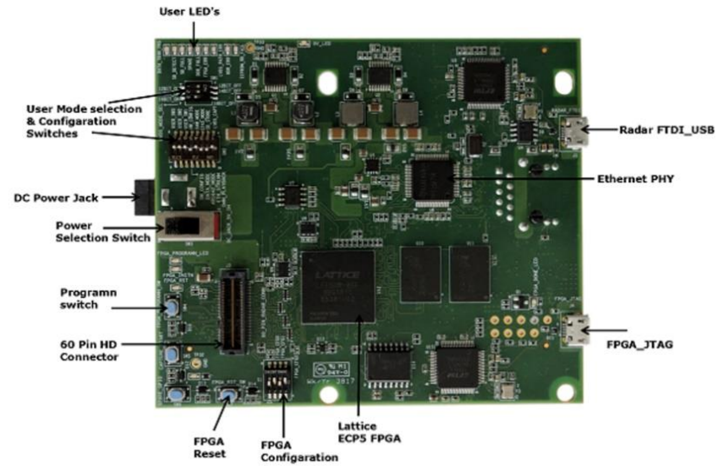


Figure 7: DCA1000EVM top side

Figure 9: DCA1000EVM and IWR1843BOOST mounted with ribbon cable connection

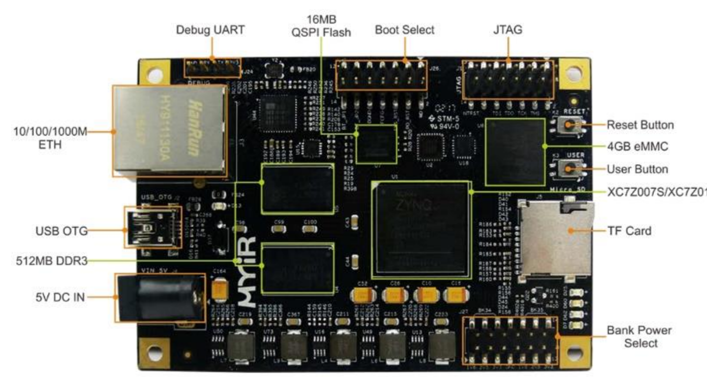


Figure 10: MYIR Z-turn Lite top side with labels

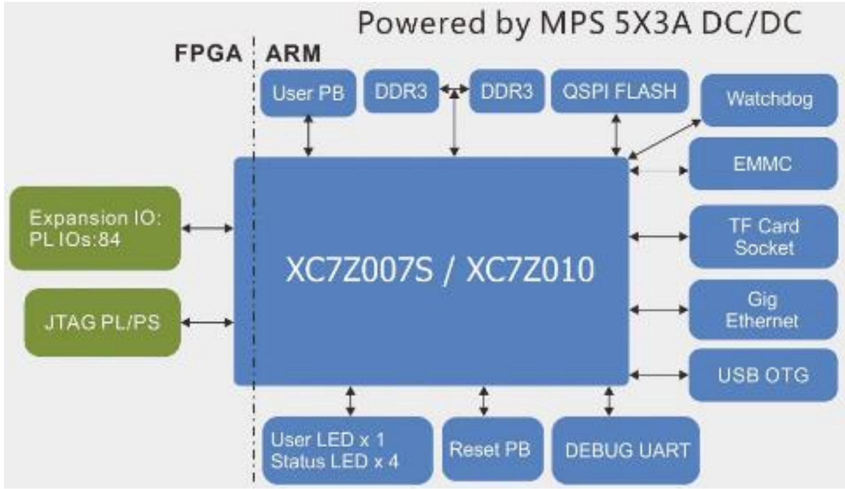


Figure 12: MYIR functional block diagram

Table 1: LCCR Bill of Materials

Item #	Part #	Manufacturer	Cost	Description	Notes
1	IWR1843BOOST	Texas Instruments	$299	Evaluation Module	[4] lists BOM for this item
2	DCA1000EVM	Texas Instruments	$499	Data Capture Card	either 2 or 2* will be used in design
2*	MYS-7Z007S-C-S	MYIR Tech Limited	$69	Data Capture Card	
3	Enclosure	SRC, Inc.	$50	3D printed Enclosure	
4	GSM40A05-P1J	Mean Well USA Inc	$23.60	5V 5A	Power Supply
5	Imposer Board	SRC, Inc	$50	Imposer	Custom Imposer Board
6	Misc Cables	Various	$50	COTS Cables	
	Total Cost including Item 2		$971.60	Category: State of the COTS Art Radars	
	Total Cost including Item 2*		$541.60	Category: Maximum Value	

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